Statement of Volatility – Overland-Tandberg Olympus O-R800

The Statement of Volatility provides you the information related to volatile and non-volatile components of different configurations of Overland-Tandberg Olympus O-R800 servers. Volatile components lose their data when power cord is removed from the system, whereas, non-volatile components continue to retain their data when the power has been removed from the component.

The following table provides information of different configurations of the Olympus O-R800 servers.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size of memory	Type of memory (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	What is the Purpose? (e.g. boot code)	How is data written to this memory?	How is memory write protected?	How is memory cleared?
Planar										
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH	256 Bytes	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings	BIOS	N/A – BIOS only control	Perform the following steps: 1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.

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Planar										
BIOS Password (part of PCH internal CMOS RAM)	Non-Volatile	1	U_PCH	16 bytes (out of 256 bytes used for PCH Internal CMOS RAM)	Battery-backed CMOS RAM	Yes	Password to change BIOS settings	Keyboard	N/A – BIOS only control	1) Place shunt on J_PSWD_NVRAM jumper pins 2 and 4. 2) AC power off is required after placing the shunt. 3) AC power on with the shunt in place and then can be removed
Primary BIOS SPI Flash	Non-Volatile	1	U_PRIM_SPI_BIOS	32MB	SPI Flash	No	Boot code	SPI interface via PCH	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	Non-Volatile	1	U_IDRAC_SPI	4 MB	SPI Flash	No	iDRAC Uboot (bootloader)	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC eMMC	Non-Volatile	1	U_eMMC	4GB	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware	NAND Flash interface via iDRAC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface

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Planar										
CPU Vcore Regulators	Non-Volatile	2	U8003, U8043	16 KB	ROM	No	Operational parameters	Programmed at factory via I2C	No write protect	Not user clearable
Vmem Regulators	Non-Volatile	2	U8011, U8051	16 KB	ROM	No	Operational parameters	Programmed at factory via I2C	No write protect	Not user clearable
System CPLD RAM	Volatile	1	U_CPLD	92Kb	FLASH	No	Not utilized	Not utilized	Not accessible	Not accessible
System CPLD FLASH	Non-Volatile	1	U_CPLD	256Kb	RAM	No	Power on System Firmware	Firmware update	BIOS Security Protocols	Not user clearable
System Memory: RDIMM and LRDIMM	Volatile	Up to 12 per CPU	CPU<2:1>_CH<5:0>_D<1:0>	Up to 128GB per DIMM	DRAM	Yes	System OS RAM	System OS	OS Control	Reboot or power down system
System Memory: NVDIMMM-N	Non-Volatile	Up to 6 per CPUs 1 and 2 (12 total in system)	CPU<2:1>_CH<5:0>_D1	16GB per NVDIMM-N	DRAM runtime (volatile) saved to NAND flash (non-volatile) on shutdown	Yes	OS addressable memory that will persist over shutdown that is accessible at DDR speed	When system initiates a Save (AC loss, shutdown, etc.), NVDIMM-N controller will transfer data from DRAM to Flash	"OS can prevent writes to DRAM/DDR at runtime in response to NFIT table.	OS addressable memory that will persist over shutdown that is accessible at DDR speed

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Planar										
System Memory: DCPMM (AEP)	Both	Up to 6 per CPUs 1 and 2 (12 total in system)	CPU<2:1>_CH<5:0>_D1	Up to 512GB per DIMM	3DXP (volatile or non-volatile based on configuration)	Yes	Memory Mode - High capacity volatile memory slightly slower than DDR App Direct - High capacity non-volatile memory for storage tiering and other applications	Accessed via system OS	OS can prevent writes to 3DXP at runtime in response to NFIT table. Encryption is available.	Using BIOS menu option, select Cryptographic Erase or Sanitize based on type of erase needed
Internal USB Key	Non-Volatile	Up to 1	J_USB_INT	Varies (not factory installed)	Flash	Yes	General purpose USB key drive	USB interface via PCH. Accessed via system OS	No write protect	Can be cleared in system OS
CPU	Volatile	1 or 2	CPU1 / CPU2	Various	Cache + registers	Yes	Processor cache + registers	Various	Various	Remove A/C
iDRAC DDR	Volatile	1	U_IDRAC9_DRAM1	512Mb	DRAM	No	iDRAC local memory	iDRAC Firmware	No write protect	Remove A/C

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Planar										
iDRAC	Volatile	1	U_IDRAC	For CPU: 128KB + Registers Co-proc: 64Kb + Registers	Cache + registers	No	Processor cache + registers	iDRAC Firmware	No write protect	Remove A/C
PIROM	Non-Volatile	1 or 2	CPU1 / CPU2	256 Bytes	EEPROM	No	Processor info + scratchpad	SMBus interface to iDRAC	128 bytes protected by Intel/128 bytes not protected	Not user clearable
Recovery BIOS SPI	Non-Volatile	1	U208	16MB	SPI Flash	No	Recovery image	SPI interface via iDRAC	No write protect	Not user clearable

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2x2.5" Rear Backplane										
SEP internal flash	Non-Volatile	1	U_SEP	Flash:64KB+ 4KB EEPROM: 2KB	Integrated Flash+EEP ROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Backplane External FRU	Non-Volatile	1	U_BP_EEPR OM	256 Bytes	I2C EEPROM	No	FRU	Programmed at ICT during production.	No write protect	Not user clearable
4x3.5" Mid Backplane										
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+ 4KB EEPROM: 2KB	Integrated Flash+EEP ROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Backplane External FRU	Non-Volatile	1	U_BP_EEPR OM	256 Bytes	I2C EEPROM	No	FRU	Programmed at ICT during production.	No write protect	Not user clearable
24x2.5" EXP/Backplane										
NVSRAM memory	Non-Volatile	1	U_NVSRAM	1 Mb	Flash	No	FW config data	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable

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Flash memory	Non-Volatile	1	U_FLASH	128 Mb	Flash	No	Firmware	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU	Non-Volatile	1	U_EXP_EEPROM	512 Bytes	I2C EEPROM	No	FRU	I2C interface via expander	Hardware strapping	Not user clearable
Backplane FRU	Non-Volatile	1	U_BP_EEPROM	256 Bytes	I2C EEPROM	No	FRU	I2C interface via iDRAC	Hardware strapping	Not user clearable
16x2.5" EXP/Backplane										
NVSRAM memory	Non-Volatile	1	U_NVSRAM	1 Mb	Flash	No	FW config data	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Flash memory	Non-Volatile	1	U_FLASH	128 Mb	Flash	No	Firmware	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU	Non-Volatile	1	U_EXP_EEPROM	512 Bytes	I2C EEPROM	No	FRU	I2C interface via expander	Hardware strapping	Not user clearable

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Backplane FRU	Non-Volatile	1	U_BP_EEPROM	256 Bytes	I2C EEPROM	No	FRU	I2C interface via iDRAC	Hardware strapping	Not user clearable
8x2.5" Backplane										
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+ 4KB EEPROM: 2KB	Integrated Flash+EEPROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
8x3.5" Backplane										
SEP internal flash	Non-Volatile	1	U_SEP	Flash:64KB+ 4KB EEPROM: 2KB	Integrated Flash+EEPROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
12x3.5" EXP/Backplane										
NVSRAM memory	Non-Volatile	1	U_NVSRAM	1 Mb	Flash	No	FW config data	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable

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Flash memory	Non-Volatile	1	U_FLASH	128 Mb	Flash	No	Firmware	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Backplane FRU	Non-Volatile	1	U_BP_FRU	256 Bytes	I2C EEPROM	No	FRU	I2C interface via expander	Hardware strapping	Not user clearable
Expander FRU	Non-Volatile	1	U_EXP_FRU	512 Bytes	I2C EEPROM	No	FRU	I2C interface via iDRAC	Hardware strapping	Not user clearable
4x2.5" Rear Backplane										
SEP internal flash	Non-Volatile	1	U_SEP	Flash:64KB+4KB EEPROM: 2KB	Integrated Flash+EEPROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Backplane FRU	Non-Volatile	1	U_BP_EEPROM	256 Bytes	I2C EEPROM	No	FRU	Programmed at ICT during production.	No write protect	Not user clearable

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H730P, H740P, H840 PERCs										
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	No write protect. Not visible to Host Processor	Not user clearable
FRU	Non-volatile	1	U1019	256B	FRU	No	Card manufacturing information	Programmed at ICT during production.	No write protect	Not user clearable
SPD	Non-volatile	1	U22	256B	SPD	No	Memory configuration data	Pre-programmed before assembly	No write protect. Not visible to Host Processor	Not user clearable
Flash	Non-volatile	1	U1086	16MB	Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	No write protect. Not visible to Host Processor	Not user clearable

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Backup Flash	Non-volatile	1	U1100	8GB	Backup Flash	No	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure	No write protect. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.
SDRAM	Volatile	9	U1077-U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	No write protect. Not visible to Host Processor	Cache can be cleared by powering off the card

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H330 PERC										
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	No write protect. Not visible to Host Processor	Not user clearable
FRU	Non-volatile	1	U1019	256B	FRU	No	Card manufacturing information	Programmed at ICT during production.	No write protect	Not user clearable
1-Wire EEPROM	Non-volatile	1	U22	256B	SPD	No	Memory configuration data	Pre-programmed before assembly	No write protect. Not visible to Host Processor	Not user clearable
Serial Boot ROM	Non-volatile	1	U1086	16MB	Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	No write protect. Not visible to Host Processor	Not user clearable
Flash	Non-volatile	1	U1100	8GB	Backup Flash	No	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure	No write protect. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.

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HBA330 PERC										
NVSRAM	Non-volatile	1	U1033	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	No write protect. Not visible to Host Processor	Not user clearable
FRU	Non-volatile	1	U1019	256B	FRU	No	Card manufacturing information	Programmed at ICT during production	No write protect	Not user clearable
Serial Boot ROM	Non-volatile	1	U1020	8KB	Serial Boot ROM	No	Bootloader	Pre-programmed before assembly	No write protect. Not visible to Host Processor	Not user clearable
Flash	Non-volatile	1	U3	16MB	Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	No write protect. Not visible to Host Processor	Not user clearable

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PCIe SSD Extender Card										
Switch Configuration EEPROM	Non-Volatile	1	U2	256B	SPI Flash EEPROM	No (requires specialized SW)	Configuration for PLX PCIe switch, setting registers	The EEPROM image is pre-loaded at factory before assembly. Once assembled on the card, data can be entered via PLX Device Editor or PLX EEP DOS based tool.	Device can be write protected via hardware pin. Alternatively, device contents can be write protected via WPEN bit in status register.	System is not functional as intended if corrupted/removed.

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Left Status Control Panel										
Microcontroller	Non-Volatile	1	U_TINY	8KB	Flash	No	Driving Health and Status LED	I2C via iDRAC	Hardware strapping	Not user clearable
Left Control Panel with Quick Sync 2										
Microcontroller	Non-Volatile	1	USAM7	32Mb	SPI Flash	No	For field maintenance. Have License, Service Tag and system information. Driving health and status LEDs	SPI interface via iDRAC	Hardware strapping	Not user clearable
TPM										
Trusted Platform Module (TPM)	Non-Volatile	1	U_TPM	128 Bytes	EEPROM	Yes	Storage of encryption keys	Using TPM Enabled operating systems	SW write protected	F2 Setup option
Right Control Panel										

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SPI Flash	Non-Volatile	1	U2	32 Mb	SPI Flash	No	EasyRestore functionality: contains Service Tag, Copy of SEL logs	SPI interface from iDRAC to Right Cntl Panel	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not user clearable,
IDSDM - vFlash										
vFlash (uSD)	non-volatile	1	J3	16GB	NAND flash	yes	populate out-of-band or optionally connect to the host as mass storage and boot mechanism	User can provide data to iDRAC (entirely in the iDRAC domain) to be pushed into vFlash	No write protect	(1) card may be physically removed and destroyed or cleared via standard means on a separate computer OR (2) User has access to the card in the host domain and may clear it manually

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iDSDM (uSD1, uSD2)	non-volatile	2	J1, J2	16GB, 32GB, 64GB	NAND Flash	Yes	Provides mass storage	device resides in host domain; they are exposed to the user via an internally connected, non-removable USB mass storage device	physical write protect switch on ACE card	(1) Card may be physically removed and destroyed or cleared via standard means on a separate computer OR (2) User has access to the card in the host domain and may clear it manually
SPI Flash	Non-Volatile	1	U2	1MB	SPI Flash	SPI flash is only indirectly connected to iDRAC. iDRAC can read any address in the SPI flash, but may only write the primary firmware storage area as a part of a firmware update procedure.	Boot firmware storage, configuration and state data for IDSDM.	User can initiate a firmware update of the IDSDM device.	There is no mechanism provided to iDRAC to write any SPI NOR area outside of the primary IDSDM firmware region.	iDRAC may issue a clear command to erase all contents of the SPI NOR, but doing this will leave the IDSDM non-functional.

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BOSS										
SPI FLASH	Non-Volatile	1	U17	1024KB	FLASH EEPROM	No	Boot code, FW	By programming the image via firmware update process	N/A	Use Flash tool, type “go.nsh w y”
TFRU	Non-Volatile	1	U7	64KB	FLASH EEPROM	Yes	Thermal monitoring	During Manufacturing, by programming the image via firmware update process. During runtime, by I2C Proprietary Command Protocol	N/A	By writing to Flash
LCD Bezel										
Microcontroller	Non-Volatile	1	IC1	256KB	Internal Flash	No	bootloader and s/w implementation of LCD command set	Updated as part of secure iDRAC software update. Configuration parameters can change only as part of iDRAC update	Writes are only allowed as part of secure iDRAC update	Not user clearable.

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PSU										
Microcontroller	Non-Volatile	Up to 3	Microchip	Up to 64KB	Flash PROM and EEPROM	Yes	Report PSU information and control firmware	The data is flash via Dell Update Package (DUP)	Using signature and manufacture key to protect memory write	Before firmware update, the memory will be clear.

NOTE: For any information that you may need, direct your questions to your Overland-Tandberg Marketing contact.